Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A microprocessor, comprising:

registers for holding values, wherein said registers are logically partitioned into register windows;

a storage for storing values held in the registers of the register windows;

a detector for detecting that a register window overflow condition or a register window underflow condition is imminent, by determining if execution of any ~~fetched instructions~~ cached instructions that are next slated for insertion into an execution pipeline will result in a register window overflow condition or a register window underflow condition; and

an instruction generator responsive to the detector for generating at least one instruction to manipulate the storage to avoid a trap ~~to avoid stalling the microprocessor, wherein the trap unconditionally performs~~ by performing, in response to the determination, at least one of a register window spill operation or a register window fill operation responsive to the condition that is detected as imminent.

2. (Original) The microprocessor of claim 1, wherein the detector and the instruction generator are implemented in hardware.

3. (Original) The microprocessor of claim 1, wherein the microprocessor further comprises a cache for caching instructions for introduction into an execution stage and wherein the detector examines the instructions in the cache to determine if a register window overflow condition is imminent by determining if execution of any of the fetched instructions will result in a register window overflow condition.

4. (Previously Presented) The microprocessor of claim 3, wherein the detector looks for an instruction in the cache that stores contents of a register window in the storage when the registers have no available space for storing the contents.

5. (Original) The microprocessor of claim 3, wherein the detector examines how much storage space is available in the registers.

6. (Currently Amended) The microprocessor of claim 1, wherein the microprocessor ~~farther~~ further comprises a cache for caching instructions for introduction into an execution stage and wherein the detector examines the instructions in the cache to determine if a register window underflow condition is imminent by determining if execution of the instructions will result in a register window underflow condition.

7. (Previously Presented) The microprocessor of claim 6, wherein the detector looks for an instruction in the cache that restores a register window when contents of the register window are stored on a stack rather than in the registers.

8. (Original) The microprocessor of claim 1, wherein the detector detects solely whether a register window underflow condition is imminent.

9. (Original) The microprocessor of claim 1, wherein the detector detects solely whether a register window overflow condition is imminent.

10. (Original) The microprocessor of claim 1, wherein the detector detects both whether a register window overflow condition is imminent and whether a register window underflow condition is imminent.

11. (Currently Amended) The microprocessor of claim 1, wherein the microprocessor ~~farther~~ further comprises an execution unit for executing the instruction generated by the instruction generator.

12. (Original) The microprocessor of claim 1, wherein the microprocessor performs out of order execution of instructions.

13. (Original) The microprocessor of claim 1, wherein the instruction generator includes a second storage for holding the at least one instruction that is generated by the instruction generator.

14.-15. (Canceled)

16. (Currently Amended) In a microprocessor having a plurality of registers logically partitioned into register windows and a storage for storing contents of register windows, a method, comprising the steps of:

determining that a register window overflow condition or a register window underflow condition is imminent by performing a logic operation on a value representative of a state of a register and a value representative of an instruction held in cache and determining if execution of any ~~fetched instructions~~ cached instructions that are next slated for insertion into an execution pipeline will result in a register window overflow condition or a register window underflow condition; and

in response to determining that the register window overflow condition or the register window underflow condition is imminent, manipulating the storage to avoid a trap by ~~unconditionally~~ performing at least one of a register window spill operation and a register window fill operation responsive to the condition determined as imminent.

17. (Previously Presented) The method of claim 16, wherein, when it is determined that a register window overflow condition is imminent, the step of manipulating the storage comprises providing at least one instruction for execution by the microprocessor that causes the contents in at least the selected register window to be stored in the storage.

18. (Previously Presented) The method of claim 16, wherein, when it is determined that a register window underflow condition is imminent, the step of manipulating the storage comprises providing at least one instruction for execution by the microprocessor that causes data in the storage to be stored in the registers.

19. (Original) The method of claim 16, wherein the microprocessor has an instruction stream slated for execution and wherein the instruction that causes the contents in at least the selected register window to be stored in the storage is inserted into the instruction stream.